

Advances in Inter-Channel Mismatch Calibration for Time-Interleaved Analog-to-Digital Converters: A Review

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Abstract

Time-interleaved analog-to-digital converters (TIADCs) increase the aggregate sampling rate by distributing conversion across several lower-rate channels. However, differences in channel offset, gain, and sampling instant introduce periodic spurs and limit the dynamic performance obtainable from interleaving. This review examines the mechanisms of individual and combined mismatches and traces the development of calibration from foreground parameter identification to background adaptation, digital reconstruction, and all-digital joint compensation. Statistical estimation, correlation-based time-skew estimation, derivative and Taylor-series compensation, adaptive filtering, and fractional-delay and filter-bank reconstruction are compared in terms of reference requirements, operating assumptions, accuracy, and implementation cost. Particular attention is given to neural-network- and machine-learning-based calibration, including nonlinear mappings, temporal features, and hybrid representations that combine physical models with learned correction. These approaches can represent coupled errors, but their usefulness depends on training-data coverage, label accuracy, out-of-distribution generalization, and the cost of continuous inference. The discussion distinguishes background parameter adaptation from the continuous application of fixed coefficients, and separates measured-data validation from real-time hardware deployment. Future research should address broadband and complex-signal robustness, explicit channel information, lightweight fixed-point implementations, and stable online adaptation. Model-data hybrid methods are a promising direction when evaluated against appropriate conventional baselines. Reliable progress ultimately requires evidence from real converters and sustained data streams, with calibration accuracy assessed jointly with throughput, latency, resource use, and power.

Keywords

Time-interleaved Analog-to-Digital Converter (TIADC); Inter-channel Mismatch; Timing Mismatch; Background Calibration; All-digital Calibration; Neural Network; Hardware Implementation.

1. Introduction

Broadband communication receivers, radar systems, electronic instruments, and high-speed data-acquisition platforms require analog-to-digital converters (ADCs) that preserve amplitude and phase over a wide input bandwidth. Raising the conversion rate of a single ADC shortens the time available for acquisition, comparison, and logic decisions. Improving resolution and linearity, in contrast, often requires larger devices, more accurate settling, or higher bias currents. Sampling rate, resolution, and power therefore form a coupled design problem that also includes input driving and clock distribution [1].

A time-interleaved analog-to-digital converter (TIADC) distributes successive samples among phase-shifted sub-ADCs and reorders their outputs into a high-rate sequence. The converter-array work of Black and Hodges established an early foundation for this approach [2].

Interleaving relaxes the conversion-time requirement of each channel, but introduces a separate consistency requirement: the channels must observe the same input with sufficiently similar offset, gain, frequency response, and sampling timing. Relative errors repeat with the interleaving cycle and generate spurs that can obscure weak signals even when the nominal sampling rate is high.

Calibration has consequently become part of the converter architecture rather than an optional output adjustment. Existing approaches differ in how they obtain mismatch information, where they apply correction, and whether they update parameters during normal operation. Neural networks add a further option by learning a correction mapping from data, although fitting capability alone establishes neither robustness to unseen conditions nor real-time feasibility. This review relates mismatch mechanisms to conventional and data-driven calibration, compares their assumptions and costs, and discusses implementation in field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs).

2. TIADC Fundamentals and Mismatch Mechanisms

2.1. TIADC Architecture and Technology Evolution

An M-channel TIADC operating at an aggregate sampling rate f_s assigns each sub-ADC a rate of f_s/M . Ideally, adjacent channels sample at intervals of $1/f_s$, and digital multiplexing reconstructs the original temporal order. Channel identity repeats every M output samples. With matched responses, accurate sampling phases, and adequate input bandwidth, the interleaved sequence is equivalent to uniformly spaced high-rate sampling, as shown in Fig. 1 [3]. Interleaving increases sampling density; it does not directly increase the quantization resolution of an individual conversion.

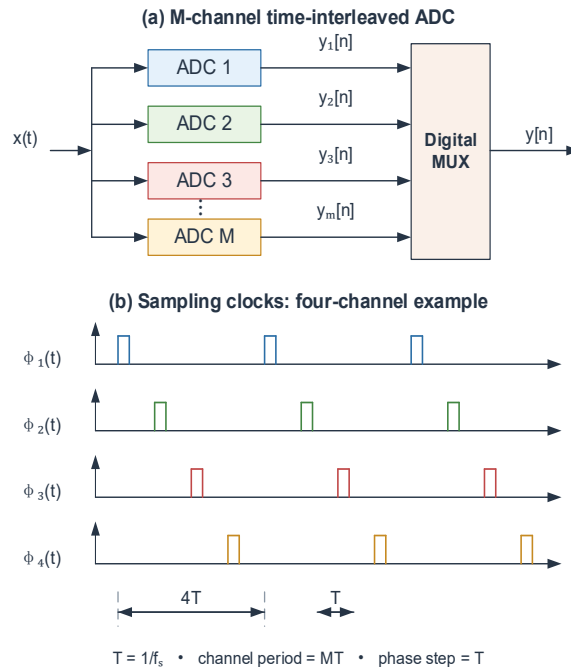


Fig 1. Architecture and interleaved sampling sequence of an M-channel TIADC.

Conceptual schematic of the architecture discussed in [3]. The digital block multiplexes the channel outputs. In the timing sketch, T_s denotes a sub-ADC period; the ideal channel spacing is $T_s/M = 1/f_s$.

The lower conversion rate of each sub-ADC does not permit its sampling network to ignore the full input bandwidth. Every channel must track the same high-frequency input, while the shared

buffer drives the aggregate sampling load. Additional channels also increase routing, clock distribution, coupling, and output-reordering costs. The interleaving factor must therefore be chosen together with the input bandwidth, converter architecture, and calibration budget, rather than by dividing a target sampling rate by an isolated sub-ADC rate.

The progression toward multi-GS/s conversion illustrates this architectural tradeoff. Alpman et al. reported a 7-bit, 2.5-GS/s interleaved successive-approximation-register (SAR) ADC in 45-nm complementary metal-oxide-semiconductor (CMOS) technology [4]. El-Chammas and Murmann combined a 5-bit, 12-GS/s flash architecture with background time-skew calibration [5]. These examples emphasize conversion efficiency and speed, respectively, while both depend on controlling the timing differences introduced by interleaving.

At tens of GS/s, input sampling and clock alignment become increasingly central. Representative developments include the 20-GS/s, 6-bit ADC with embedded time-to-digital calibration reported by Chen and Pileggi [6], and the 46-GS/s, 6-bit ADC with hierarchical interleaving and sparkle-code correction reported by Duan and Alon [7]. Kull et al. described 36- and 90-GS/s implementations for 100-Gb/s communication applications, emphasizing the interaction between input bandwidth, track-and-hold timing, and clock paths [8]. Increasing the interleaving factor alone is insufficient at these rates; analog bandwidth and digital assistance must be optimized together.

Research by teams in China also spans channel-level circuits and system-level correction. Chan et al. reported a four-way, 6-bit, 5-GS/s interleaved SAR ADC [9], followed by an eight-way, 7-bit, 8-GS/s implementation with attention to input linearization and sampling-buffer design [10]. Lan et al. combined a four-way, 2.5-GS/s ring-amplifier-based pipelined-SAR architecture with digital background calibration and optional neural-network calibration [11]. Collectively, these developments show a transition from improving individual conversion paths toward joint optimization of the analog front end, clocking, and digital correction.

The reported converters serve different bandwidth, resolution, and application targets. Their sampling rates should not be read as a single ranking of overall performance. Ultra-high-rate converters with moderate resolution coexist with architectures intended for more accurate broadband measurement. Across these application classes, calibration requirements extend beyond offset and gain matching to timing, frequency-response differences, and nonlinear behavior.

2.2. Inter-Channel Mismatch Mechanisms

Offset mismatch arises from comparator offsets, front-end direct-current (DC) shifts, and differences in channel operating points. Under a fixed-offset model, each channel contributes a different additive constant. The resulting periodic offset sequence produces components at $k f_s/M$, with alias folding applied when interpreting the observed spectrum. A common offset mainly changes the DC level; relative offsets produce interleaving-related spurs whose locations do not move with input frequency. Estimation from channel means is inexpensive, but becomes biased when the input contains DC, is synchronized with the interleaving pattern, or is observed over an insufficient record. Calibration must distinguish genuine offset differences from differences in the sampled signal statistics.

Gain mismatch is a periodic amplitude scaling caused by differences in capacitor ratios, amplifier gains, or reference voltages. Multiplication by the periodic channel-gain sequence translates the input spectrum. For a sinusoidal input at f_{in} , characteristic images occur at $k f_s/M \pm f_{in}$, interpreted modulo the aggregate sampling rate and folded into the displayed band. Common gain error changes absolute amplitude calibration, whereas relative gains create interleaving images. Variance or power estimates can support gain normalization when all channels sample comparable input distributions. Offsets should be removed first, and a

constant gain factor should not be expected to correct frequency-dependent bandwidth mismatch.

Timing mismatch originates in clock-path delays, sampling-switch behavior, and differences in effective front-end delay. For sufficiently small time skew, the induced amplitude error is approximately proportional to the product of the skew and the input derivative. At a fixed sinusoidal amplitude, a higher input frequency therefore produces a larger error for the same skew. Periodic timing errors generate spectral images at the interleaving translation frequencies illustrated conceptually in Fig. 2 [3]. These images may coincide with those caused by gain mismatch, so a spur magnitude at one frequency does not uniquely identify its physical cause.

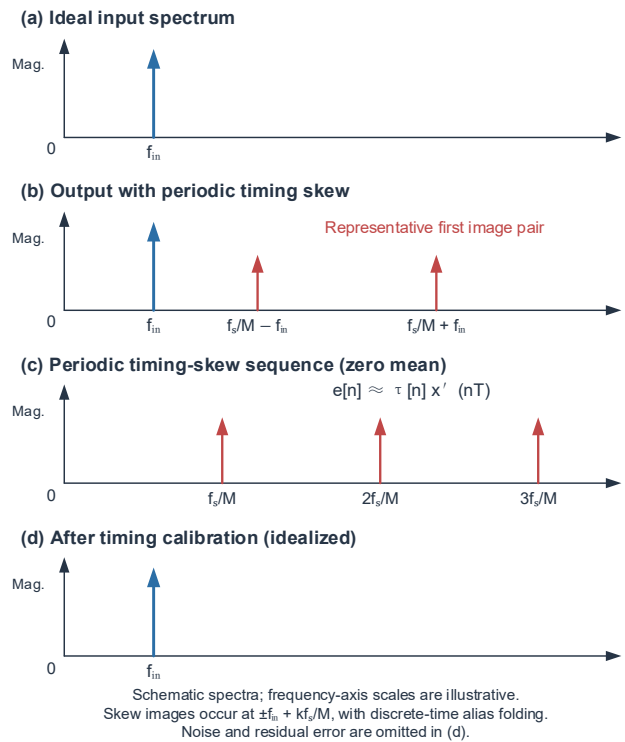


Fig 2. Spectral translation and spur-generation mechanism induced by timing mismatch in a TIADC.

Conceptual illustration based on [3]: (a) ideal input; (b) output with time skew; (c) periodic mismatch modulation; (d) idealized corrected spectrum. The axes are qualitative; image locations follow $k f_s/M \pm f_{in}$, with alias folding.

Deterministic time skew must be distinguished from random clock jitter. Fixed or slowly varying channel offsets have repeatable structure that an estimator can track. Unpredictable sampling fluctuations generally contribute noise or phase noise and cannot be removed sample by sample using fixed correction coefficients. Similarly, a common delay shifts the overall time reference, whereas relative delays disturb the spacing of the interleaved sequence. At high input frequencies, residual skew, derivative-estimation error, and random clock uncertainty can all limit performance; calibration must therefore accompany an appropriate low-jitter clock design.

Real converters contain several mismatch sources simultaneously. Gain differences alter correlation magnitudes, bandwidth differences change adjacent-sample relationships, and these effects can bias a timing estimator. Compression, clipping, and nonlinear memory further restrict the validity of a linear mismatch model. Joint calibration is needed when these interactions matter, but does not necessarily require one large compensator. Separable errors can be corrected in stages, with iterative or joint updates introduced when the residuals of one

stage influence another. Reference constraints are necessary to distinguish relative channel matching from absolute amplitude and phase calibration. Digital processing cannot restore information already lost through saturation.

3. Evolution of TIADC Calibration Techniques

3.1. Conventional Calibration Approaches

Conventional approaches are best classified along three separate dimensions: operating mode, source of mismatch information, and compensation structure. Foreground and background describe when estimation occurs; reference-assisted and blind describe how the estimator obtains information; analog adjustment and digital reconstruction describe where correction is applied. These categories overlap. A digital filter, for example, can use parameters identified either during an initial calibration interval or continuously during operation.

Foreground calibration applies a controlled DC, sinusoidal, or multitone stimulus before normal acquisition. Known conditions simplify identification of offset, relative gain, and time skew, and permit relatively costly optimization during initialization. This is useful when a measurement system allows startup or maintenance intervals. Its weakness is the difference between calibration conditions and actual operation. A single-frequency adjustment need not capture broadband response, and fixed coefficients may become inaccurate as temperature or supply voltage changes. Multidimensional characterization and interpolation improve coverage at the cost of test time and storage. Continuously applying coefficients obtained beforehand is continuous compensation, but is not background parameter adaptation.

Background calibration updates mismatch estimates while the converter processes its intended input. The analog and digital background techniques reported by Dyer, Fu, Lewis, and Hurst illustrate that the correction action may reside on either side of the analog-digital boundary [12, 13]. Jamal et al. subsequently demonstrated digital background calibration in a 10-bit, 120-Msample/s interleaved converter [14]. The central change was to incorporate estimation into normal operation rather than rely entirely on one-time characterization. Background operation nevertheless has costs: a reference or redundant channel requires circuitry, injected excitation consumes signal margin, and blind estimation relies on properties of the input.

Offset and gain correction are comparatively mature because their compensation structures are simple. Subtracting a channel-dependent mean and applying a scale factor require few arithmetic operations. Recursive averaging reduces record storage, and slow parameter updates can be separated from the high-rate sample path. The estimator remains conditional, however. Long observation windows reduce statistical uncertainty but respond slowly to drift; short windows may mistake an input-envelope change for gain variation. Practical implementations also require protection against low signal energy, bounded updates, and careful handling of divisions or reciprocals to avoid new modulation artifacts.

Timing correction can act directly on the sampling clock through variable-delay elements or phase adjustment. Correcting the sampling position before quantization reduces the burden on subsequent reconstruction, and background timing correction is part of the broader interleaved-converter design problem discussed by Razavi [1]. Residual accuracy depends on adjustment range, delay resolution, added jitter, and process or environmental drift. These limitations motivate digital alternatives, although digital processing does not remove the need for adequate analog sampling quality.

Derivative and Taylor-series methods estimate the amplitude error caused by time skew and subtract it from the measured sequence. A first-order model is attractive for small skew. Near the band edge or for larger offsets, higher-order terms and differentiator approximation errors become relevant. Raising the expansion order can improve model fidelity, but higher derivatives amplify sensitivity to noise and finite word length. The coarse-and-fine strategy

studied by Xiong et al. addresses higher-order timing errors and illustrates this accuracy-complexity tradeoff [3]. The derivative path and the skew estimator must be evaluated together; an accurate correction formula cannot compensate for a systematically biased parameter estimate.

Correlation-based estimators exploit changes in statistical relationships between adjacent samples or selected channels. They can track slow skew in the background without a dedicated training waveform under specific input conditions. Their error signals also depend on the input power spectrum and other mismatches. Salib et al. examined a low-complexity correlation approach and its blind-estimation constraints [15]. When the relevant correlation structure degenerates, or signal content overlaps a mismatch image, an estimator may be unable to separate useful signal from error. Auxiliary excitation, controlled sampling arrangements, or update-freezing rules may then be necessary.

The least-mean-squares (LMS) algorithm and related adaptive methods specify how parameters are updated; they are not separate physical models of mismatch. They can operate with derivative compensation, reference-channel observations, or blind correlation objectives. A large step size accelerates initial adaptation but raises steady-state fluctuations and may destabilize the loop. A small step size limits tracking speed. Strongly correlated inputs and coupled parameters can also create unequal convergence rates. An adaptive scheme therefore needs a defined objective, initialization strategy, and excitation conditions rather than an assumption that adaptation works for arbitrary input data.

Digital reconstruction treats the channel outputs as samples of a nonideal sampling system. Finite-impulse-response (FIR) filters, fractional-delay filters, and multichannel filter banks approximate the desired uniformly sampled sequence. Johansson and Löwenborg studied reconstruction of nonuniformly sampled bandlimited signals using digital fractional-delay filters [16]. Filter order depends on usable bandwidth, transition width, and allowable approximation error. A narrow transition band or stringent residual target generally increases both arithmetic and delay.

Perfect reconstruction is a property obtained when the signal model and reconstruction filters satisfy the required conditions. It does not imply that a finite-order, quantized circuit recovers every input without error. Model uncertainty, noise gain, coefficient quantization, and record boundaries all contribute residuals. Polyphase decomposition distributes computation across lower-rate branches, as illustrated by the digital feedforward background method of Le Duc et al. [17]. It eases clock-rate requirements but does not eliminate the aggregate operations, memory traffic, or interbranch exchange. Filter order, parallelism, and storage bandwidth must be designed as a coupled implementation problem.

3.2. All-Digital and Joint Calibration

All-digital calibration places mismatch estimation and sample correction primarily in digital circuitry, enabling configurable parameters and algorithm updates. Its development has expanded from separate offset and gain adjustment toward timing, frequency-response, and joint-error correction. Analog, mixed-signal, and all-digital approaches nevertheless coexist because they address different constraints. Qiu et al. investigated all-digital blind background calibration for an arbitrary interleaving-channel configuration [18], extending the scope of digital methods without removing their input-dependent identifiability requirements.

Joint calibration can use several small estimators updated sequentially or alternately, or optimize multiple parameters under a common objective. Ta et al. combined mean estimation, power-ratio calculations, and Hadamard-transform/LMS processing to correct offset, gain, and timing mismatches, with numerical simulation as the validation basis [19]. Staged structures simplify resource allocation and interpretation, but require analysis of interstage coupling. Unified optimization can control the overall residual while introducing correlated parameters

and longer convergence. A common reference is still required if the goal includes absolute gain or delay rather than relative channel consistency alone.

Fig. 3 illustrates the functional separation of offset estimation, gain estimation, time-skew estimation, and joint digital compensation. It relates to the background-calibration concept and optional neural correction discussed by Lan et al. [11]. The estimator paths obtain slowly varying parameters, whereas the correction path processes every output sample. The optional learned branch represents an additional compensation choice; it does not by itself imply that its weights are updated during normal acquisition.

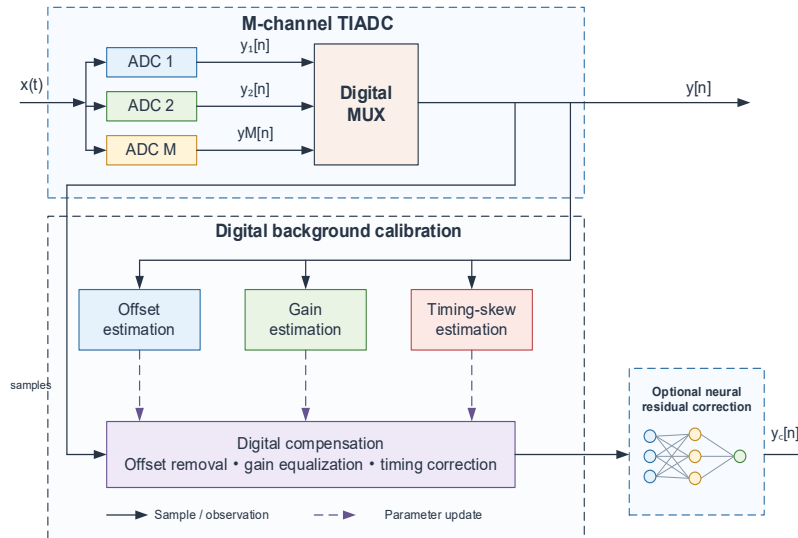


Fig 3. Digital background joint calibration framework for offset, gain, and timing mismatches in a TIADC.

Conceptual schematic based on the calibration concept in [11]. Estimation paths update the digital compensator; neural correction is optional. The drawing summarizes functions rather than a complete circuit implementation

Digital implementation offers portability and reconfiguration through coefficient changes, but its high-rate path must meet the sustained input data rate. A low-rate estimator can reduce update cost without relaxing the throughput requirement of a sample-by-sample compensator. High-order filters and joint optimization still consume multipliers, registers, and on-chip memory. The benefit of digital integration must therefore be weighed against the amount of parallel arithmetic and data movement needed for a particular converter rate.

All-digital compensation also need not be reference-free. Zhong et al. used a reference channel to support timing estimation and correction of differentiator error, evaluating both a converter model and off-chip processing of commercial-converter data [20]. Fig. 4 shows the associated conceptual organization. The reference supplies additional observations of the input, while correction remains in the digital domain. Reference quality, sample alignment, scheduling, and the cost of the extra channel remain part of the architecture. Selection should separately consider the information source, compensation location, required tracking behavior, and signal bandwidth.

4. Neural-Network- and Machine-Learning-Based Calibration

4.1. Development of Data-Driven TIADC Calibration

Parametric calibration is effective when the relevant errors can be identified and represented compactly. Coupled mismatch, nonlinearity, and memory can make that representation harder

to obtain. A neural network can instead learn a mapping from corrupted samples to a target output, or predict a residual correction added to or subtracted from the original signal. Both formulations require accurate input–target alignment. Residual prediction retains a direct signal path and focuses the learned function on the error, but does not remove the need for reliable training information.

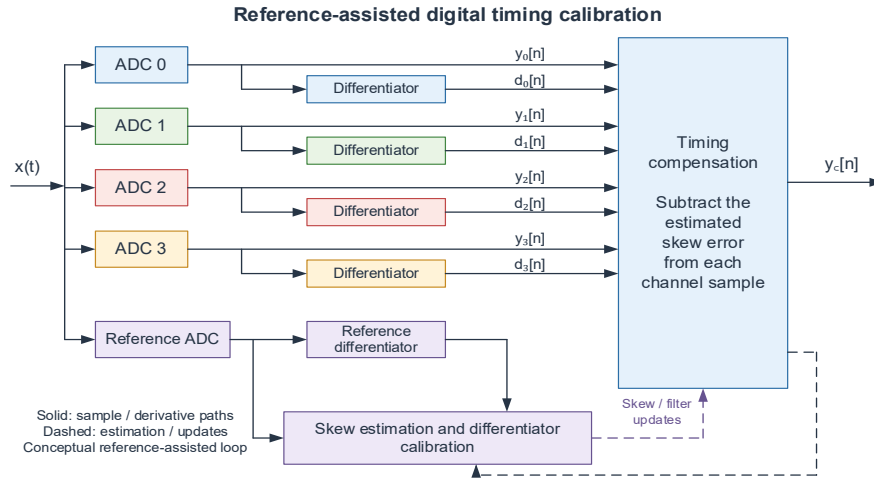


Fig 4. Reference-channel-based all-digital timing-mismatch calibration architecture. Conceptual schematic based on the reference-channel calibration strategy in [20]. The differentiators support time-skew compensation, and the auxiliary path addresses differentiator error.

Qiu et al. investigated neural-network-based correction of gain and time-skew mismatches [21], providing an example of the transition from explicit parameter compensation to learned mappings. The target remained recognizable channel mismatch, while the network reduced the need to construct a separate analytical compensator for each error. Training coverage still determines which input and mismatch conditions can be represented. A learned mapping therefore replaces part of the explicit modeling task with a data-design task rather than eliminating prior assumptions.

The scope broadened in the additive-neural-network work of Zhai et al., which addressed nonlinear amplitude and phase distortion in high-speed and time-interleaved ADCs [22]. This extends the objective beyond suppression of interleaving images to distortion within the conversion paths. Evaluation must consequently distinguish changes in harmonics, interleaving spurs, and noise floor. An improvement in one aggregate spectral metric does not establish which error mechanism was removed.

Ware et al. connected neural calibration with an eight-channel, 6-GS/s SAR TIADC prototype [23]. Such work moves the evidence beyond idealized mismatch simulations and toward actual converter behavior. The converter chip, acquisition arrangement, and execution platform of the neural network remain separate aspects of the experiment, however. Calibration of measured data does not alone demonstrate that the network runs on the converter chip or sustains the complete conversion rate in deployed hardware.

Bhanushali et al. explored machine-learning-based blind digital calibration using a two-channel TIADC test chip in 28-nm CMOS [24]. A low-rate, high-accuracy ADC provided reference information for supervised learning of static and dynamic errors. In this context, blind calibration refers to avoiding prior identification of particular error sources, rather than eliminating reference hardware or training labels. This distinction matters when comparing area, power, and system applicability with conventional blind statistical estimators.

Model-assisted learning offers a further development. Liu et al. combined a learned Volterra polynomial with a lightweight neural network for joint nonlinear-distortion and mismatch calibration of time-interleaved pipelined ADCs, and evaluated the approach using real converter data [25]. A structured nonlinear representation can account for part of the response, leaving a compact network to model additional relationships. Fig. 5 summarizes this hybrid concept. The scientific question is not merely whether a network improves a spectrum, but whether the selected representation reduces learning and implementation demands while retaining performance over relevant operating conditions.

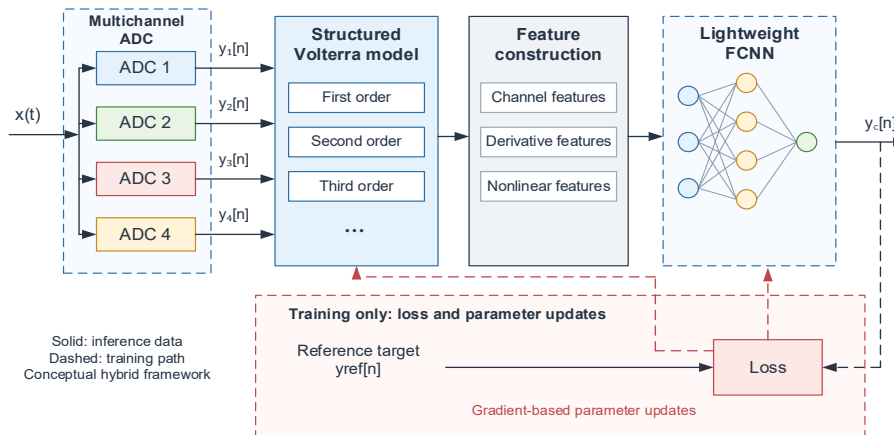


Fig 5. Hybrid Volterra–neural-network framework for joint nonlinear-distortion and mismatch calibration.

Conceptual schematic based on the hybrid calibration approach in [25]. Structured Volterra terms and learned features support a lightweight fully connected neural network (FCNN); the lower path represents training against a target output.

These developments illustrate the potential of a common learned function to represent coupled errors, although that potential is constrained by the information supplied to it. A single sample amplitude may be insufficient to distinguish channels with different error laws or signals with different local slopes. Temporal context can reveal local dynamics, while channel identity or sampling phase can distinguish otherwise similar samples. Such features also increase buffering, arithmetic, and synchronization requirements. Their usefulness should be demonstrated through controlled comparisons with compact conventional baselines, not inferred from network size or the improvement over uncalibrated data alone.

4.2. Challenges in Neural Calibration

Training-data coverage and label accuracy are central limitations. Simulation provides convenient ideal targets but can omit coupling, reference fluctuations, and memory effects in real circuitry. Measured data capture these effects more faithfully, yet their targets may contain signal-generator distortion, reference-ADC errors, or timing misalignment. A network can learn these target errors as readily as converter errors. Low training loss is therefore insufficient evidence of accurate signal recovery. Data provenance should record the stimulus, converter conditions, and reference chain so that the meaning of the learned correction remains traceable. Generalization requires evaluation across input frequency, amplitude, mismatch range, temperature, and device instance. Testing an unseen sinusoidal frequency supports a narrower conclusion than testing multitone, modulated, or nonstationary inputs. Temporal windows create a further risk: randomly splitting overlapping windows can place many of the same raw samples in both training and test sets. Independent acquisition records, operating conditions, or chips should define the data split, with explicit out-of-distribution tests. Performance should

also be checked when the input has weak excitation or spectral content similar to the targeted mismatch artifacts.

Deployment cost includes more than the number of learned parameters. Weights determine only part of storage demand; sample windows, intermediate activations, memory access, and control can dominate a streaming implementation. Fixed-point quantization can also affect small residuals disproportionately. Accumulator overflow, inconsistent scaling, rounding bias, and saturation may create new spurs even when the floating-point model appears accurate. Word lengths should be selected using the actual signal and residual ranges, and calibration quality should be reevaluated after quantization rather than inferred from floating-point inference.

Real-time throughput is a distinct requirement from processing a finite record quickly on a general-purpose computer. An FPGA or ASIC must accept and produce samples at the required sustained rate while respecting memory bandwidth and latency constraints. Reusing arithmetic units reduces area but can lengthen the initiation interval. Deep pipelines improve timing closure while increasing registers and latency. Temporal models that use future samples also incur an unavoidable look-ahead delay. A credible deployment study should account for all these costs, including interfaces and sample reordering.

Online adaptation requires a stable source of supervisory or self-supervisory information. A fixed network can compensate continuously, but its weights cannot track a new operating condition without an update mechanism. Unconstrained updates may degrade previously calibrated behavior or suppress legitimate changes in the signal. Drift detection, bounded updates, validation before coefficient replacement, and recovery to known parameters are therefore relevant design considerations. Limited interpretability further motivates residual monitoring and a bypass path: distribution shift, clipping, and channel synchronization faults should not all be treated as reasons to enlarge the model.

5. Comparative Assessment and Future Directions

5.1. Comparison of Calibration Techniques

Table 1 compares representative approaches by their correction targets, information requirements, background capability, and implementation burden. The rows are not mutually exclusive categories: foreground calibration is an operating mode, FIR filtering is a compensation structure, and LMS is an update mechanism. Complexity labels are qualitative and assume broadly comparable channel counts, signal bandwidths, and accuracy targets. They do not replace counts of operations, word lengths, memory accesses, or measured power.

The comparison highlights how calibration trades controlled information against estimation assumptions and computation. Foreground identification simplifies the problem through a known stimulus but requires calibration intervals. Statistical offset and gain estimation reduces reference overhead when channel statistics are comparable. Correlation methods can track time skew, but become unreliable when their input-dependent error signal loses sensitivity. Derivative/Taylor methods expose the timing-error mechanism directly, whereas adaptive filtering supplies the update process needed to follow changing coefficients.

Fractional-delay FIR and perfect-reconstruction methods provide systematic frequency-domain control at the cost of filter order, latency, and coefficient precision.

All-digital joint calibration extends correction to interacting errors while adding parameter coupling and data-path cost. Neural-network calibration transfers part of model construction to data collection and training; it does not eliminate the cost of obtaining trustworthy targets or demonstrating the operating range. Useful combinations include foreground initialization of

background estimators, linear correction followed by learned residual compensation, and reference-assisted model updates.

Table 1. Comparison of representative TIADC mismatch calibration techniques

Calibration method	Target mismatch	Reference requirement	Back-ground capability	Computational complexity	Hardware complexity	Main advantages	Main limitations
Foreground parameter calibration	Offset, gain, timing	Known stimulus	No; calibration interval	Low to medium	Low to medium	Direct estimation; useful initialization	Calibration interval; limited drift tracking
Statistical estimation	Offset, gain	Usually no external reference	Conditional	Low	Low	Simple arithmetic; slow update path	Comparable statistics; sufficient record length
Correlation-based calibration	Mainly timing	Blind or auxiliary information	Conditional	Low to medium	Medium	Tracks slowly varying skew	Input-dependent sensitivity; confounding errors
Derivative / Taylor-series compensation	Timing	Depends on skew estimator	With online estimation	Medium	Medium	Physical error model; staged correction	Truncation and differentiator errors
LMS / adaptive filtering	Depends on objective and filter	Reference or blind objective	Conditional	Medium	Medium	Iterative adaptation; drift tracking	Step size, excitation, and coupling affect convergence
FIR / fractional-delay filtering	Timing, frequency response	Response or skew parameters	With online estimation	Medium to high	Medium to high	Controlled in-band approximation	Order, word length, latency, and resource cost
Perfect reconstruction / filter banks	Timing, frequency response	Model or parameters	With online estimation	Medium to high	High	Unified multichannel reconstruction	Ideal conditions do not ensure exact finite-order recovery
All-digital joint calibration	Multiple mismatch types	Architecture-dependent	Conditional	Medium to high	Medium to high	Configurable; coupled-error correction	Parameter coupling; high-rate data-path cost
Neural-network / machine-learning calibration	Mismatch; nonlinear errors	Usually labels or reference information	Requires an online update mechanism	Depends on model	Often high	Nonlinear mappings; temporal and channel features	Data coverage, generalization, quantization, deployment

Background capability denotes the availability of in-operation estimation or parameter updates. Continuous execution with fixed coefficients alone is not background adaptation. Methods may be combined; complexity levels are qualitative.

Method selection should begin with observability and operating conditions. Stable equipment that permits interruptions may need only periodic parameter calibration. Continuous systems with suitable input statistics can benefit from background estimation. Broadband dynamic errors may justify reconstruction filters, while coupled nonlinearities may justify neural correction when representative data are available. Accuracy must be assessed alongside

tracking speed, latency, power, and resource use. Spurious-free dynamic range (SFDR), signal-to-noise-and-distortion ratio (SNDR), and effective number of bits (ENOB) provide complementary information under specified measurement conditions; a favorable single-tone SFDR result is not a complete system assessment.

5.2. Future Research Directions

Joint calibration should address offset, gain, timing, and bandwidth mismatch while separating relative channel differences from distortion common to all channels. Reference constraints, staged initialization, and sensitivity analysis can reduce ambiguity between parameters. Testing should vary the combinations of errors, because suppressing the initially dominant mechanism can reveal a different performance limit. Broadband robustness also requires band-edge, multitone, and varying-envelope inputs. Estimators should be checked for inadvertent removal of useful components when signal spectra overlap interleaving images. Amplitude response, phase response, noise floor, and application-level metrics should accompany SFDR and SNDR.

Lightweight design must reduce arithmetic, storage, and data movement together. Conventional filters can exploit coefficient symmetry, constant-coefficient multiplication, polyphase organization, and staged compensation. Neural methods can investigate structured pruning, shorter temporal windows, low-rank representations, and quantization-aware training. Their value should be measured in a concrete implementation: fewer nominal operations do not necessarily translate into fewer digital signal processing (DSP) blocks, less memory, or lower power. Irregular sparsity may introduce control and access costs that offset arithmetic savings.

FPGA-oriented evaluation should report input parallelism, operating clock, and initiation interval, since these jointly determine sustained throughput. Multibank block random-access memory (BRAM) can increase concurrent access but adds allocation and boundary-management overhead. Pipeline latency, window look-ahead, and output reordering should be included in the end-to-end delay. ASIC evaluation additionally requires process, area, and power conditions. A useful verification progression compares floating-point and fixed-point behavior, checks fixed-point samples against register-transfer-level (RTL) results, evaluates synthesis and post-layout timing, and then tests uninterrupted board-level streams. Functional simulation, a generated bitstream, and stable operation on hardware establish different levels of evidence.

Hybrid model-driven and data-driven calibration can assign well-understood errors to compact analytical structures while reserving a small network for residual behavior. This may reduce model size and training requirements, but must be demonstrated under common datasets, accuracy targets, and hardware budgets. Ablation studies should identify whether gains arise from the physical representation, temporal features, or the network itself. Explicit channel identity is particularly relevant because TIADC outputs have a known periodic origin. Channel-conditioned parameters, shared models, and residual learning are plausible directions, subject to the cost of feature encoding and cross-channel processing.

Temporal windows and channel labels must remain synchronized with the actual acquisition sequence. Channel reordering, missing samples, or a change in acquisition mode can invalidate this association. Their handling belongs in the hardware architecture as well as the learning model. Online methods may limit adaptation to a small set of channel coefficients or output-layer weights, reducing update cost and exposure to unstable learning. Reference-assisted targets, spectral constraints, or application-derived error signals can support adaptation under their respective assumptions. Update triggers, freezing criteria, recovery rules, and drift-response time should be evaluated together; suspending updates may be preferable during weakly excited or transient inputs.

Finally, validation should extend across converters, temperatures, supply conditions, and independent acquisition sessions, with traceable raw and reference data. Simulation, post-processing of chip measurements, and real-time hardware calibration should be reported separately. Shared datasets containing complex signals, drift trajectories, and implementation constraints would improve reproducibility and comparability. The long-term objective is reliable acquisition under changing conditions, with calibration assessed through energy, maintainability, and continuous operation as well as spectral improvement.

6. Conclusion

TIADCs raise the aggregate conversion rate through interleaving, but relative offset, gain, and timing errors limit the dynamic performance of the combined sequence. Calibration has developed from foreground characterization toward background tracking, digital reconstruction, all-digital joint correction, and data-driven compensation. These approaches continue to coexist because they rely on different combinations of controlled references, input statistics, response models, and training data. No method is uniformly preferable across accuracy, adaptability, throughput, hardware complexity, and power requirements.

Neural networks expand the available representations for coupled mismatch and nonlinear distortion, while introducing obligations in data quality, generalization, quantization, and deployment. Hybrid physical and learned models, explicit channel structure, and lightweight streaming architectures are promising directions when supported by appropriate comparisons. Progress should be demonstrated through reproducible converter measurements and sustained hardware operation, so that improvements in a calibration metric translate into dependable high-speed acquisition.

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