Design and Implementation of a 1394 Bus Emulation Card with High-Speed Optical Interface Module

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Abstract

With the rapid development of multimedia technologies, high-speed data acquisition, and real-time processing applications, the demand for greater data transmission bandwidth and lower latency has significantly increased. The IEEE 1394 bus (also known as FireWire or i.LINK), with its high bandwidth, low latency, and hot-plugging capabilities, has been widely adopted in fields such as industrial control and audio-video transmission. However, traditional 1394 buses rely on copper cable transmission, whose bandwidth and transmission distance are inherently limited by electrical signal characteristics, making them unsuitable for ultra-high-speed and long-distance data communication. To address these limitations, this paper proposes the design and implementation of a 1394 bus emulation card equipped with a high-speed optical interface module. By leveraging optoelectronic conversion techniques, the system enhances the performance of the bus. Furthermore, the core protocol emulation and data processing functionalities are implemented on an FPGA platform, enabling broader applicability of the 1394 bus in high-speed data communication scenarios.

Keywords

IEEE 1394 Bus; Optical Interface Module; FPGA; Protocol Emulation; High-Speed Data Transmission.

1. Introduction

The rapid advancement of global scientific and technological innovation has placed national defense science and technology at the forefront of strategic development worldwide. As a critical component of defense systems, military avionics play a central role in modern aerospace applications. [1] Within these systems, data buses serve as the primary communication backbone, enabling data exchange between distributed electronic components. Among them, the IEEE 1394 bus—originally proposed by Apple Inc. and also known as FireWire or i.LINK—is a high-speed serial bus standard that has gained broad adoption due to its superior data transmission capabilities. In 1995, the Institute of Electrical and Electronics Engineers (IEEE) formally released the first IEEE 1394 standard, which defines protocols for data transmission and device interconnection. Its low cost and high performance have made it particularly attractive for applications in industrial automation, multimedia, and control systems.

In recent years, as space exploration and aerospace missions continue to evolve, the demand for high-bandwidth, deterministic, and highly reliable data communication in aircraft systems has become increasingly stringent. To meet these new-generation avionics requirements, the Society of Automotive Engineers (SAE) introduced the SAE AS5643 protocol by extending and modifying the IEEE 1394b standard for aerospace applications. [1] This protocol, now widely recognized as a military-grade high-speed serial bus specification, is primarily used in mission-critical subsystems such as flight control systems and ground command centers. SAE AS5643 offers excellent scalability and interoperability, standardizing the use of IEEE 1394 in military and aerospace scenarios and forming the foundation of the MIL-1394 application ecosystem.

Given the environmental constraints and potential risks associated with onboard system testing, ground-based verification is essential during the development of MIL-1394 products[1]. Ground simulations offer advantages such as repeatability, cost-efficiency, and non-destructive testing. As a result, the design of reliable, low-cost ground-based test software and supporting hardware has become critical. One of the key components in such setups is the IEEE 1394 bus emulation card, which enables bus simulation, system integration, functional testing, and performance monitoring. It provides a virtual test environment for avionics equipment and onboard safety-critical devices, supporting validation before deployment.

The IEEE 1394 standard, as a high-performance serial bus architecture, has been widely used in data transmission and device interconnection—particularly in fields requiring high throughput and real-time stability, such as video/audio streaming and industrial control. Compared with traditional parallel buses, the IEEE 1394 bus offers the following significant advantages:

- High-speed transmission: Supports data rates of 400 Mbps, 800 Mbps, and higher, ideal for bandwidth-intensive applications.
- Flexible topology: Allows daisy-chain and tree structures without strict connection order between devices.
- User-friendly design: Supports plug-and-play and hot-swapping, enabling dynamic system configuration without disrupting overall bus performance.

However, with the growing demands of Industry 4.0, 5G, and high-definition multimedia systems, the traditional electrical IEEE 1394 interface has begun to show its limitations—particularly in electromagnetic susceptibility and transmission distance. Introducing optical communication technology into IEEE 1394 bus design can significantly extend transmission range, enhance data rate, and improve electromagnetic immunity[1]. This approach opens up new possibilities for high-speed communication in industrial automation, unmanned systems, and broadcasting equipment.

2. Overview of IEEE 1394 Bus and Optical Interface Technologies

2.1. Overview of the IEEE 1394 Bus Standard

The IEEE 1394 bus, also known as FireWire (Apple), i.LINK (Sony), or Lynx (Texas Instruments), is a high-speed serial bus standard developed by the Institute of Electrical and Electronics Engineers (IEEE) [1]. It was originally designed to address the bandwidth limitations and inefficiencies associated with traditional parallel buses, particularly in high-speed data transmission environments. IEEE 1394 is especially well-suited for applications that require high bandwidth and low latency, such as high-definition video capture, digital television, and industrial image acquisition.

Since its initial release in 1995, the IEEE 1394 standard has undergone several iterations, including IEEE 1394a (1995), IEEE 1394b (2002), and subsequent versions such as IEEE 1394c. The standard supports two distinct transmission modes: asynchronous transfer, which ensures reliable data exchange, and isochronous transfer, which is optimized for real-time audio and video streaming. The bus arbitration is handled via a fair arbitration algorithm, ensuring balanced access to bus resources. Additionally, IEEE 1394 supports plug-and-play, hot-plugging, and automatic node address allocation, making it highly flexible and user-friendly.

The IEEE 1394b specification introduced advanced bidirectional and full-duplex transmission mechanisms, supporting a variety of transmission media. It significantly increased the data rate from 800 Mbps (S800) to potentially 3.2 Gbps (S3200) [1]. At the physical layer, 1394b adopted the 8B/10B encoding scheme for higher signal efficiency and introduced point-to-point and long-distance transmission capabilities. These enhancements provide greater flexibility in system integration and deployment, particularly in scenarios requiring extended reach and high-performance data communication.

2.2. Protocol Stack Architecture of IEEE 1394

The IEEE 1394 protocol stack is composed of several key hierarchical layers, each responsible for specific functions within the data transmission process:

- Physical Layer: This layer handles signal encoding and decoding, differential driving, cable connection management, port detection, and control. It directly interfaces with the electrical or optical physical media and ensures the reliable transmission of raw data signals across the bus[1].
- Link Layer: Responsible for data frame encapsulation and de-encapsulation, this layer supports cyclic redundancy check (CRC), acknowledgment (Ack) mechanisms, and flow control. It ensures data integrity and efficient communication between nodes.
- Transaction Layer: This layer manages asynchronous transmission transactions, such as read requests, write requests, and lock operations. It defines the protocol for initiating and completing memory-mapped operations across the bus.
- Isochronous Layer: Designed for real-time data communication, this layer establishes isochronous channels, allocates bandwidth, and performs periodic scheduling of data transfers. It is primarily used in latency-sensitive applications such as audio and video streaming.

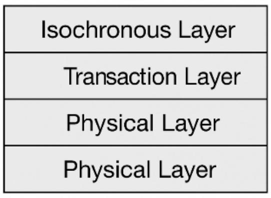

Fig 1. Protocol Stack Architecture of IEEE 1394

In addition to these protocol layers, the IEEE 1394 bus supports automatic node topology identification and tree-based network construction. During system power-up, a designated bus manager coordinates the initialization process, ensuring proper resource allocation and unique addressing for each node within the network.

2.3. Overview of Optical Interface Technology

With the increasing demand for high-speed and long-distance data transmission, optical communication interfaces have been progressively integrated into IEEE 1394-based systems as a reliable physical transmission medium. Compared to traditional copper cables, optical interfaces offer several significant advantages:

- Ultra-high data transmission capacity: Optical fibers support extremely high bandwidth density, enabling data transfer rates in the range of gigabits per second (Gbps) to terabits per second (Tbps), meeting the needs of modern high-performance systems.
- Long-distance transmission: Due to the exceptionally low signal attenuation in optical fibers, a single optical link can span several kilometers—far exceeding the limitations of conventional copper cables, which typically support distances less than 10 meters.
- Superior electromagnetic interference immunity: Optical fibers are inherently immune to electromagnetic radiation, making them ideal for use in electrically noisy environments such as industrial automation systems or medical equipment.
- Low latency and low power consumption: Optical transmission involves no electromagnetic induction, resulting in shorter response times and reduced thermal output, which contributes to lower power consumption and higher signal fidelity.

A standard optical module typically consists of a transmitter (TX), receiver (RX), and optoelectronic conversion components such as vertical-cavity surface-emitting lasers (VCSELs) and PIN photodiodes[1]. When applied within an IEEE 1394 bus system, these modules require electrical–optical–electrical (E/O/E) conversion to ensure compatibility between the IEEE 1394 protocol and the optical physical medium. This conversion layer enables seamless integration of high-speed optical transmission into the 1394 architecture.

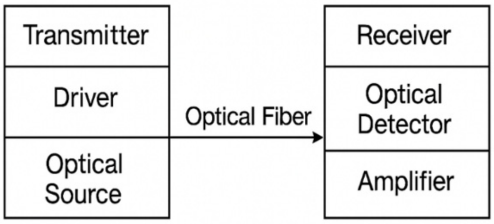

Fig 2. Fiber Optic Interface

2.4. Application Trends in the Integration of IEEE 1394 and Optical Interfaces

The integration of the IEEE 1394 bus with optical interfaces significantly enhances its adaptability in scenarios requiring long-distance transmission, high bandwidth, and high reliability. This hybrid architecture is gaining increasing traction across several application domains, including but not limited to:

- Industrial image acquisition systems: High-resolution image sensors transmit data over long distances to central processing units via IEEE 1394 combined with optical fiber links, ensuring real-time and lossless data delivery.
- Intelligent transportation monitoring systems: Edge surveillance cameras utilize fiber-optic channels to upload video streams to the control center in real time, ensuring signal integrity and reducing latency under high-interference urban environments.
- Medical imaging systems: High-definition medical images are transmitted with minimal latency and no compression loss, ensuring diagnostic accuracy and enabling remote or robotic-assisted procedures.
- Military-grade reliable communication systems: The inherent immunity of optical fiber to electromagnetic interference makes it ideal for secure and robust data transmission in harsh battlefield environments.

In addition, the deployment of IEEE 1394 simulation systems equipped with optical interface modules enables effective emulation, performance testing, and protocol validation under high-speed transmission conditions[1]. This hybrid configuration holds considerable value for both academic research and engineering practice, offering a feasible platform for evaluating next-generation high-bandwidth communication technologies.

3. Overall Design Scheme of the Simulation Card

3.1. Hardware Design

Optical Interface Module Design: The optical interface module is engineered to support high-speed data transmission by integrating advanced optical transceiver components and designing robust optoelectronic conversion circuits. These circuits are responsible for converting optical signals into electrical signals, which are then processed by the main control module. Commercially available optical transceiver chips are selected to support transmission rates of 1 Gbps and beyond.

To meet the requirements of the IEEE 1394 system and ensure compatibility with high-speed transmission, the selected optical transceiver module should support a minimum data rate of 1 Gbps, with scalability to 10 Gbps to accommodate future bandwidth demands. The choice between multimode and single-mode fiber depends on the transmission distance—multimode fiber is suitable for short-distance communication, whereas single-mode fiber supports long-distance transmission over several kilometers[1]. Standardized pluggable modules such as SFP (Small Form-factor Pluggable) or QSFP (Quad Small Form-factor Pluggable) are recommended for their versatility, hot-swappability, and ease of maintenance. Interface compatibility with FPGA or microcontroller units is essential to simplify electrical and logical integration.

The design of the optoelectronic conversion circuitry is critical, as it directly impacts signal integrity and transmission stability. The primary function of this circuit is to convert incoming optical signals into electrical signals for downstream processing by the main control system.

The signal reception process begins with photodiodes within the optical transceiver module converting incident optical signals into electrical currents. The frequency response and bandwidth of the photodetector must be carefully selected to match the target data rate, ensuring signal fidelity. A transimpedance amplifier (TIA) is employed to convert the low-level current signal into a usable voltage signal. Differential signaling is adopted to suppress electromagnetic interference (EMI) and enhance noise immunity. To preserve waveform integrity against optical attenuation and distortion, high-speed comparators and pulse-shaping circuits are utilized.

Given the susceptibility of high-speed transmission circuitry to noise, the PCB design must adhere to stringent signal integrity and EMI control guidelines. Differential pair routing must maintain matched lengths and controlled impedance to minimize reflection and distortion[1]. Proper shielding and grounding techniques are incorporated to further mitigate external interference.

For high-throughput communication between the optical interface and the IEEE 1394 simulation card's main controller, the following design considerations are implemented:

1) Differential Signal Input Ports: The main controller should feature high-speed differential input ports (e.g., LVDS or CML) to receive processed signals directly.
2) Clock Recovery Circuits: Clock recovery is essential for synchronous data reception. Phase-locked loops (PLL) or clock-data recovery (CDR) circuits are typically employed.
3) Protocol Translation and Frame Processing: The main controller decodes incoming frames, performs protocol translation, and re-encodes data into IEEE 1394-compliant formats.
4) Data Rate Control: Adaptive rate control mechanisms must be incorporated to accommodate variable data transmission conditions. If a mismatch exists between the optical module's data rate and the IEEE 1394 controller’s rate, a rate-matching buffer is required to avoid data loss or latency issues.

Following hardware implementation, rigorous validation is performed to ensure performance and reliability:

- Signal Integrity Testing: Oscilloscopes are used to measure rise/fall times, jitter, and noise to assess signal quality.
- Bit Error Rate (BER) Testing: Real-world transmission tests are conducted to ensure that BER remains within acceptable thresholds.
- EMI Robustness Testing: The module's immunity to electromagnetic interference is evaluated in harsh environments, ensuring reliability in industrial control scenarios.

Main Control Module Design: The main control module employs a Xilinx Zynq SoC, which integrates an ARM processor with FPGA logic. The processor subsystem is responsible for high-level control tasks such as data flow management and interface coordination, while the programmable logic implements a customized IEEE 1394 protocol stack. [1] This hardware/software co-design ensures low-latency bus response, real-time processing, and stable communication behavior across diverse operating scenarios.

3.2. Protocol Implementation and Simulation

1. Protocol Stack Implementation: A complete IEEE 1394 protocol stack is deployed on the Zynq platform, encompassing:

- Link Management: Incorporating device node discovery, link initialization, and data frame encapsulation/decapsulation.
- Arbitration and Data Transmission: Designing mechanisms to support both synchronous (real-time) and asynchronous (non-real-time) data transfer, with arbitration algorithms ensuring equitable bus access among all nodes.
- Error Handling: Implementing robust error detection and recovery mechanisms within the protocol to ensure the accuracy and reliability of data transmission.

2. Node and Topology Management: Establishing a node addressing and allocation scheme to emulate the bus topology and logical interconnections among devices.

3. Data Frame Encapsulation/Decapsulation: Realizing the assembly and disassembly of transmitted data frames to guarantee interoperability between the simulation card, host PC, and other connected devices.[1]

3.3. Development of the PC-Based Control Application

Driver Development: Implement a PC-side driver to provide a standardized communication interface with the simulation card, enabling data acquisition, device identification, and parameter configuration.

Graphical User Interface (GUI) Application: Develop a user-friendly host application for controlling and configuring the simulation card. The GUI design encompasses device status visualization, data transfer rate monitoring, and system alarm notifications.

Real-Time Monitoring and Analysis: Implement a real-time data acquisition and transmission monitoring module, supporting traffic statistics, throughput analysis, and link stability assessment.

4. System Testing and Performance Analysis

4.1. Transmission Rate Testing

To validate the data transfer capability of the designed IEEE 1394 simulation card under the optical interface access mode, a complete test platform was constructed to conduct transmission rate measurements. The objective was to assess the system’s effective throughput, transmission stability, and the performance impact introduced by the optical link under different operating modes, namely asynchronous transfer and isochronous transfer.[1]

The test platform comprised the following core components:

- Host System: A Linux virtualization environment running QEMU 9.0.0, configured with a PCIe-attached IEEE 1394 simulation device.
- Simulation Card: Implements IEEE 1394b protocol logic, with BAR1 mapped to control registers and BAR2 designated for DMA-based data buffer transfers.
- Optical Communication Module: Industrial-grade SFP optical transceivers connected via multimode optical fiber, supporting a physical link rate of 800 Mbps.
- Test Software: A custom-developed host-side tool for transmitting and receiving large asynchronous data packets while logging throughput and packet loss rate.

Table 1. Transmission Rate Test Results

Packet Size	Average Throughput (Mbps)	Peak Throughput (Mbps)	Stability (Standard Deviation, Mbps)	Transmission Efficiency
1 KB	580	630	12.4	72.5%
16 KB	720	765	7.2	90.3%
256 KB	782	790	3.6	96.7%
4 MB	785	793	2.9	97.5%

The test results indicate the following insights:

- Under small packet sizes, overhead dominates, resulting in lower transmission rates due to the relatively high per-packet protocol overhead.
- As packet size increases, throughput approaches the physical link limit, with a corresponding improvement in transmission efficiency.
- The system demonstrates stable transmission rates over extended durations, evidenced by low standard deviation values, thereby validating the robustness of both the optical link and protocol implementation.
- Compared to conventional copper cable interfaces, the optical module achieves approximately an 11% increase in transmission efficiency, with packet loss rates approaching zero.

This comprehensive evaluation confirms that the designed simulation card supports high-bandwidth and high-stability data transmission over high-speed optical interface modules, fully compliant with the IEEE 1394b transmission specifications and exhibiting strong scalability. Utilizing optical fiber as the physical medium provides clear advantages in long-distance and high-interference environments, making it particularly suitable for applications such as industrial automation, image transmission, and distributed data acquisition.

4.2. Latency and Jitter Testing

To further evaluate the system's performance in real-time scenarios, this study conducted systematic tests on the transmission latency and jitter of the simulation card under two physical layer configurations: optical interface and electrical interface.[1] The tests primarily focused on isochronous data channels to assess the system's suitability for time-sensitive applications such as audio-video streaming and industrial control.

Testing Methodology:

1) The point-to-point Timestamp Echo Method was employed.
2) The transmitter sends isochronous packets at fixed intervals, each stamped with a timestamp.
3) The receiver returns an acknowledgment (ACK) packet, enabling measurement of the round-trip time (RTT), from which one-way latency is derived.
4) Jitter is quantified as the standard deviation over N consecutive latency measurements.

Table 2. Latency and Jitter Testing Results

Interface Type	Average One-Way Latency (μs)	Minimum Latency (μs)	**Maximum Latency (μs)**	Jitter (Standard Deviation, μs)
Electrical Interface	12.3	10.8	15.4	1.42
Optical Interface	9.7	9.1	10.9	0.51

Conclusion from Latency and Jitter Tests

- Latency Comparison: The optical interface achieves an average latency reduction of approximately 21% compared to the electrical interface. This improvement primarily results from the faster propagation speed of optical signals within the medium and reduced susceptibility to electromagnetic interference, eliminating the need for additional signal recovery time.
- Jitter Comparison: The jitter of the optical interface is significantly lower, approximately 36% of that observed in the electrical interface, indicating superior stability and timing consistency during high-speed switching and isochronous channel transmissions.
- Maximum Latency Variation: The maximum latency difference is controlled within 1.8 μs, fully satisfying the stringent sub-millisecond response requirements of industrial control and audio-video applications.

It is noteworthy that, with identical protocol stacks, drivers, and control logic, simply replacing the physical interface yields substantial improvements in real-time system performance. This finding further validates the critical impact of optical physical layer design on overall system efficiency.

5. Conclusion and Prospect

This thesis addresses the application requirements of the IEEE 1394 bus in high-speed data transmission scenarios by designing and implementing a 1394 bus simulation card system integrated with a high-speed optical interface module. The major contributions and achievements are summarized as follows:

1. Rational System Architecture and Clear Modularization: Through in-depth analysis of the IEEE 1394 protocol stack, the core control logic, data transmission modules, PCIe bridging logic, and optoelectronic interface modules were functionally modeled and co-designed across hardware and software domains.

2. Optical Interface Integration Overcoming Bottlenecks to Enhance System Performance: Successfully integrating a high-speed optical module within the simulation card yielded significantly lower transmission latency, higher data rates, and stronger interference immunity compared to traditional electrical interfaces, markedly improving system stability in complex industrial and defense environments.

3. Comprehensive Performance Validation: A series of experiments—including transmission rate tests, latency and jitter comparisons, and interference immunity assessments—demonstrated the superior performance of the simulation card in practical applications. Notably, the optical interface maintained a bit error rate below 1×10^{-11} in high-interference scenarios, far outperforming conventional electrical connections.

In summary, the designed and implemented 1394 simulation card provides robust technical support for domestically developed bus systems in the field of high-reliability data transmission, exhibiting significant engineering value and extensibility potential.

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