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Design of Ultrasonic Excitation Circuit based on Half-Bridge Circuit

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Abstract

The excitation circuit of ultrasonic probe is the key and core part of the ultrasonic testing system. It ensures that the ultrasonic probe can work normally. It is a challenging design in ultrasonic testing technology, and its design quality affects the resolution and accuracy of the testing system. The piezoelectric crystal in the ultrasonic probe emits ultrasonic wave by piezoelectric effect to realize the conversion of voltage signal and stress signal. The waveform parameters of ultrasonic wave are positively correlated with the waveform parameters of voltage excitation signal. The same echo signal acts on the piezoelectric crystal to generate voltage signal to realize ultrasonic wave detection. In ultrasonic testing, due to the difference between the acoustic impedance of the tested workpiece and the coupling agent, the loss is large in the transmission process. The design goal of this design: Based on half-bridge circuit and bootstrap circuit, a pulse voltage transmitting circuit with low power consumption and adjustable pulse width and frequency parameters is developed. High voltage pulse, square wave pulse and sharp pulse excitation are often used in ultrasonic probe. This design focuses on the excitation of high voltage pulse.

Keywords

Ultrasonic Testing; Piezoelectric Effect; High Voltage Pulse; Half Bridge Circuit; Bootstrap Circuit.

1. Introduction

With the upgrading of China's high-end manufacturing industry, China's steel plate ultrasonic testing system also puts forward higher requirements for the excitation circuit, mainly including high-voltage and high-speed performance, reliability, intelligence and cost [1]. For the penetration of thick plates, the output pulse amplitude is more than 300V, and the rise time is 2nS, so as to ensure the layered defect detection of 80～150mm thick plates. Required by industrial environment, it is resistant to high temperature (-20～85$^{\circ}C$) and electromagnetic interference. Cost demand requires low cost [2]. At present, China is based on discrete circuits (silicon-based MOSFET/IGBT), and its typical output is ±100～150V with a rise time of 5～10nS. The GB/T 2970 standard thick plate requires ± 250V. European and American enterprises use customized ASIC and wide band gap semiconductor, and its typical output is high-speed pulse with an amplitude of ±400V/0.8ns [3]. In this contrast, the basic circuit in China is approaching maturity, but there is still a certain gap for high-voltage pulse excitation.

Under this background, a 200V pulse excitation circuit based on half bridge circuit and bootstrap circuit is proposed, which can promote the development of the industry to a certain extent, and has certain significance for the ultrasonic testing system of steel plate in China. [4]

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2. Simulation

Half bridge circuit is one of the basic and commonly used topologies in power electronics. It is usually composed of two MOSFETs or IGBTs in series. By controlling the conduction time and duty cycle of each triode, the corresponding pulse voltage can be output [5]. As shown in the figure. HO is upper tube control conduction signal, LO is lower tube control conduction signal, when the upper tube is conduction, 200V voltage is connected to the load ultrasonic probe to generate ultrasound; When the lower tube is connected, the load stops and the ultrasonic wave cannot be generated. The schematic diagram of half bridge circuit is shown in Figure 1.

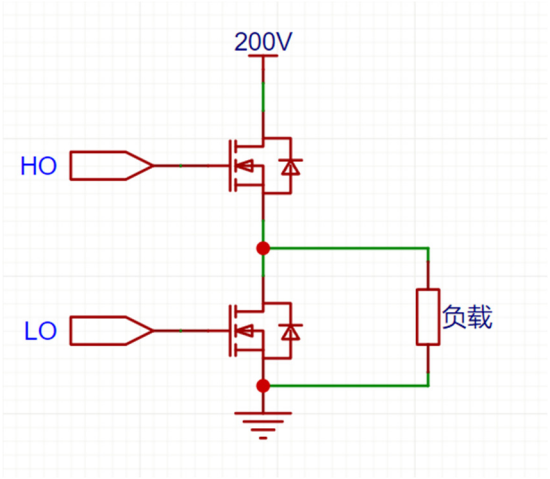

Figure 1. The schematic diagram of half bridge circuit

Due to the delay between the on/off states of MOSFET, it is necessary to avoid short circuit caused by simultaneous conduction.

Considering the above problems, the MOSFET selected in this experiment is IXTQ52N30P-JSM generated by JEMSEMI, and the parameters of this MOSFET are shown in the table 1.

Table 1. the parameters of IXTQ52N30P-JSM

Definition	Drain-Source Breakdown Voltage(V)	Gate-Source Threshold Voltage Max(V)	Turn-on Delay Time (ns)	Turn-on Rise Time (ns)	Turn-off Delay Time (ns)	Turn-off Fall Time(ns)	Gate-Source Charge(nC)
Symbol	V_{DSS}	$V_{GS(\mathrm{th})}$	$t_{d(on)}$	t_r	$t_{d(off)}$	t_f	Q_g
Value	300	4	53	65	689	230	244

In the circuit simulation, IR2112SPBF gate drive chip produced by Infineon was selected for the experiment. The parameters of this chip are shown in the table 2, and the Figure 2 shows his sequence logic diagram. HIN/LIN controls HO/LO respectively. When SD signal is low, input HIN/LIN is equal to output HO/LO; When the SD signal is high level, the output HO/LO is low level.

Table 2. The parameters of IR2112SPBF

Definition	High Side Floating Supply Voltage(V)	High Side Floating Supply Offset Voltage (V)	Turn-On Propagation Delay (ns)	Turn-Off Propagation Delay (ns)	Turn-On Rise Time (ns)	Turn-Off Fall Time (ns)
Symbol	V_B	V_S	t_{on}	t_{off}	t_r	t_f
Value	-0.3 ~ 625	V_B-25 ~ V_B+0.3	125	105	80	40

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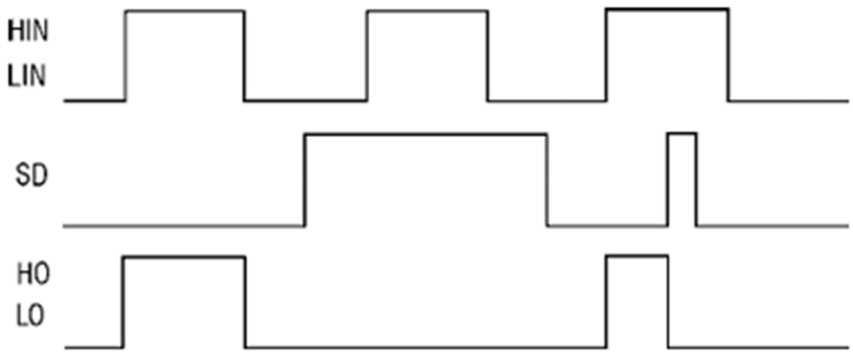

Figure 2. Sequence logic diagram of IR2112SPBF

When the SD signal is low, the chip starts to work. The output HO/LO controls the gate of the MOSFET to control the on-off of the MOSFET, and applies a voltage of 15V to the bootstrap capacitor C_4 between V_B and V_S. The working principle of bootstrap capacitor: when LO outputs high level and HO outputs low level, the lower tube is turned on and the upper tube is turned off, and 15V voltage starts to charge the bootstrap capacitor; When HO outputs high level, when LO outputs low level, the upper tube is turned on, the lower tube is turned off, and the voltage of 200V is turned on to V_S. At this time, the bootstrap capacitor is charged to 15V when the lower tube is turned on. V_B is internally connected to Ho, so V_{GS} can still maintain the voltage difference from 15V to $V_{GS(\text{th})}$. The size of bootstrap capacitor should ensure that it can provide enough energy to drive the upper tube to turn on. The size of bootstrap capacitor should be at least 10 times larger than the grid capacitance of the upper tube. The bootstrap capacitance is calculated as follows

$$C_g = \frac{Q_g}{V_{Q_{1g}}}$$

$$V_{Q_{1g}} = V_{DD} - V_{BootDiode}$$

$$C_{boot} \geq 10 \times C_g$$

The voltage drop of diode 1N4007 is 1.1V, V_{DD} is 15V, Q_g is 244nc. The calculated value of C_g is 17.6nf, C_{boot} at least 176nf. In the simulation, the bootstrap capacitor selection of 4.7uF meets the design conditions.

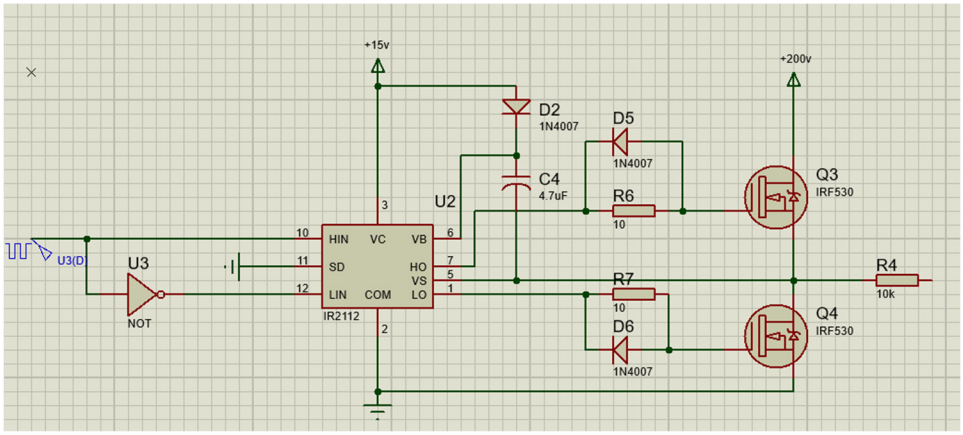

Figure 3. Circuit Simulation Diagram

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The input signal is pulse signal with frequency of 100Hz and amplitude of 5V, and a reverser is added to input the forward and reverse signals to HIN and LIN respectively. Figure 3 is the circuit simulation diagram, and Figures 4 and 5 are the waveform diagrams of the simulation results. The output result is a pulse signal with 10mS, 300uS rise time and 200V amplitude.

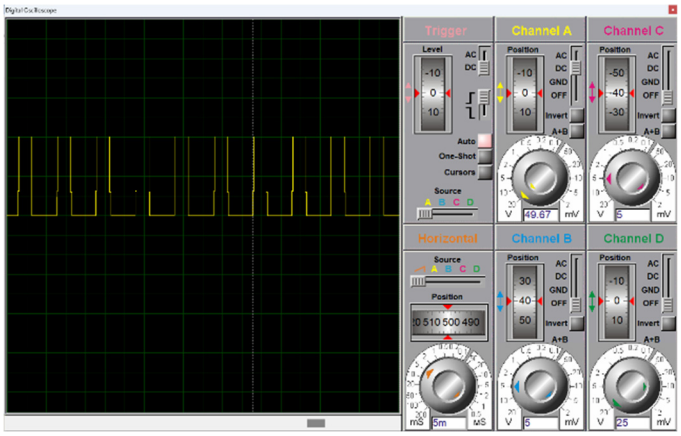

Figure 4. Output waveform(1)

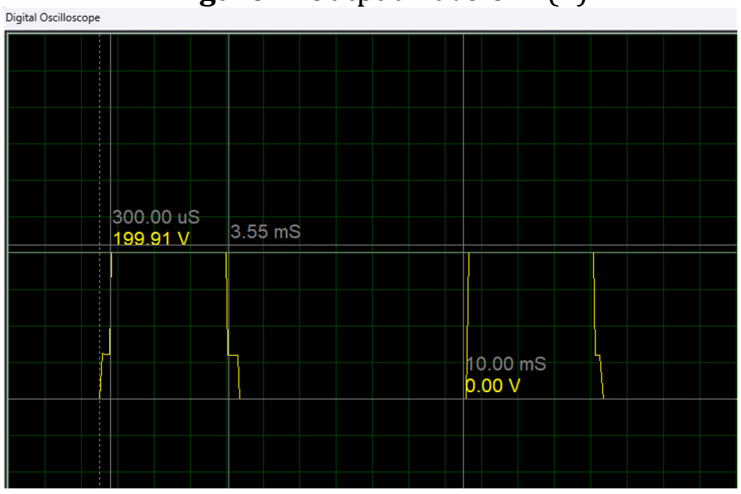

Figure 5. Output waveform (2)

3. Test

3.1. Circuit Theory

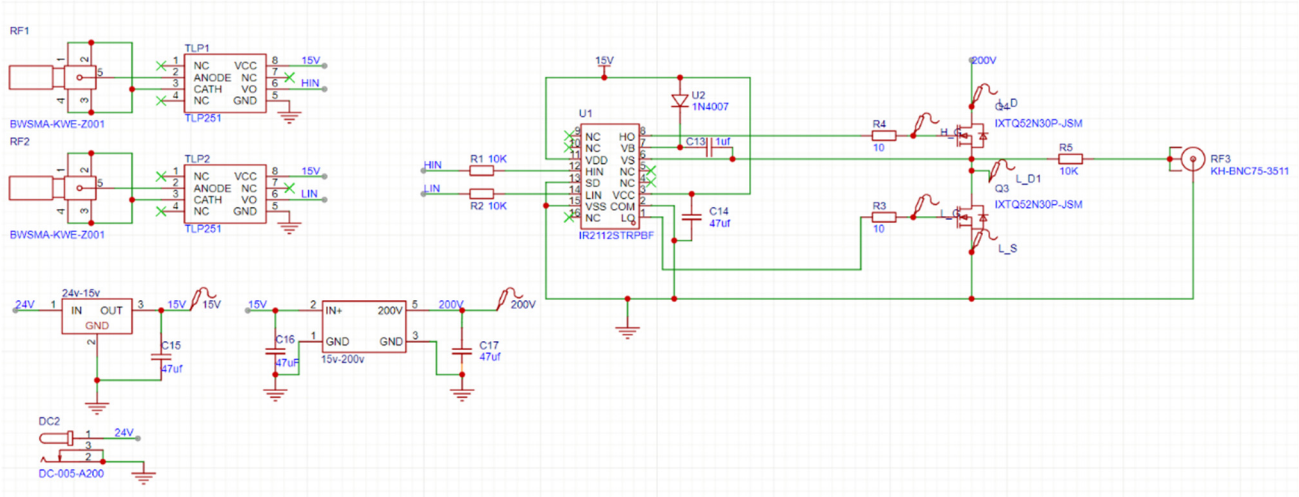

Figure 6. Circuit schematic diagram

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In the implementation circuit, TLP251 produced by Toshiba and L7815C2T linear regulator produced by STMicroelectronics and DC-DC boost module produced by Nengda. Tlp251 is to isolate the input signal from the rear circuit, because the rear high-voltage signal will affect the input signal and even cause current reflux to burn the signal generation module. L7815C2T depressurizes the input 24V power supply to 15V to provide power for TLP251 and IR2112.The DC-DC boost module boosts the 15V signal to 200V, and then connects 200V to the drain stage of the upper tube. Figure 6 is the circuit schematic diagram and Table 3 shows tlp251 parameters.

Table 3. The parameters of TLP251

Definition	Supply voltage(V)	Supply current(mA)	Operating frequency (kHz)	Input current,On (mA)	Input voltage,off (V)
Symbol	V_{CC}	I_{CC}	f	$I_{\mathrm{F(on)}}$	$V_{F(OFF)}$
Value	15	11	25	8	0.8

The input signal is generated by FPGA with a frequency of 100Hz,and the dead band is set to 80ns.In the dead band of 80ns,both the upper and lower tubes are in the cut-off state and will not burn the MOSFET. Figure 7 shows the physical connection diagram, Figure 8 is the simulation diagram of input signal, Figures 9 and 10 show the simulation diagram of input signal dead band

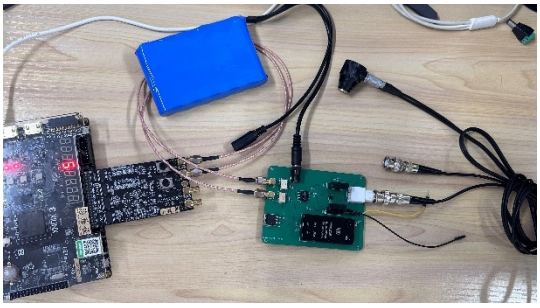

Figure 7. the physical connection diagram

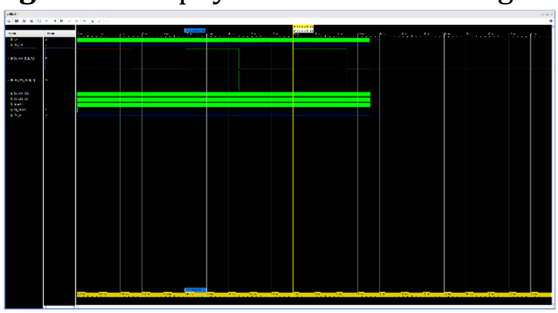

Figure 8. simulation diagram of input signal

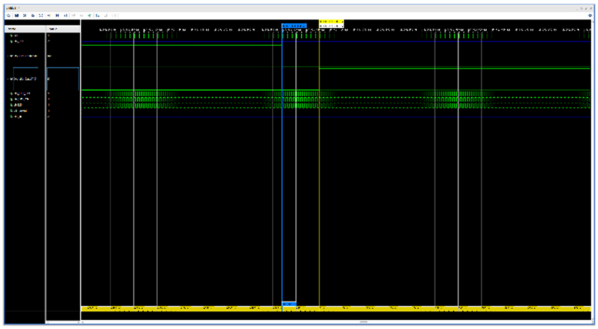

Figure 9. simulation diagram of input signal dead band(1)

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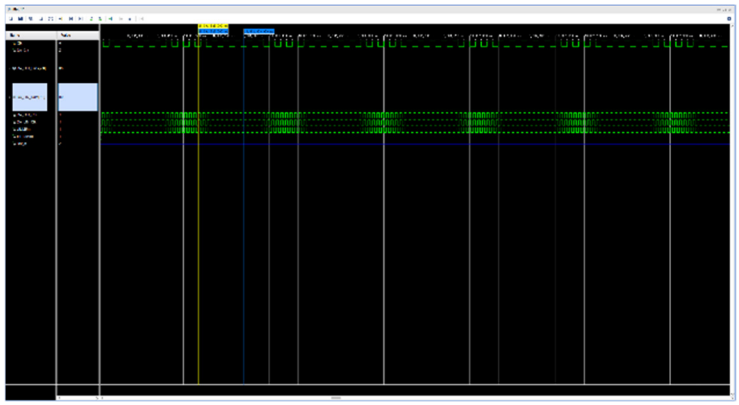

Figure 10. simulation diagram of input signal dead band (2)

The probe selected in this experiment is a bicrystal probe.Two piezoelectric crystals are placed in one probe, one is used to generate ultrasonic wave, and the other is used to receive ultrasonic signal. The parameters of the ultrasonic probe are shown in the table4

Table 4. The parameters of probe

Center Frequency(MHz)	Withstand voltage range (V)	Bandwidth(MHz)	Pulse width (ns)	Repetition rate (Hz)
5MHz	50～300V	0.5～20MHz	50～500ns	10～1000Hz

3.2. Experiment and Waveform

As shown in the figure 11, the input signal used is a pulse signal with a frequency of 100Hz,Figure 12, and the dead zone is 80ns,Figure 13 and Figure 14. Then the output 200V pulse signal is connected to one end of the probe, and the other end is connected to the oscilloscope to detect the steel plate. The oscilloscope can collect the ultrasonic return signal, which proves the design. Figure 15 shows that the echo signal and input signal are both 100Hz. Figure 16 shows the first echo signal from the top and bottom of the steel plate. Figure 17 shows two echo signals. Because of the transmission and refraction of ultrasonic wave in the steel plate, there is amplitude attenuation

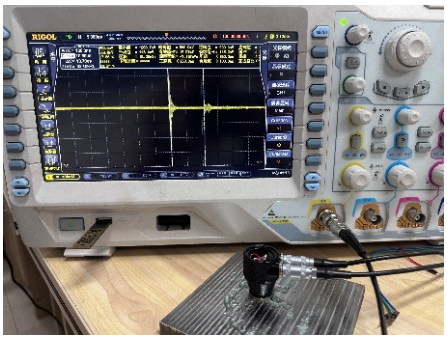

Figure 11. The input signal used is a pulse signal with a frequency of 100Hz

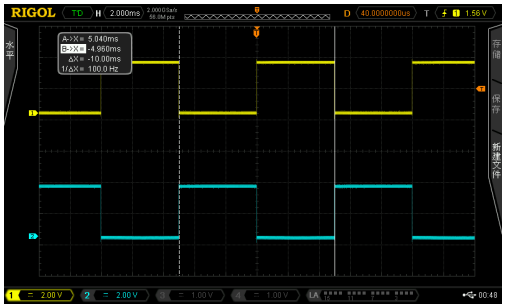

Figure 12. 100Hz waveform of input signal

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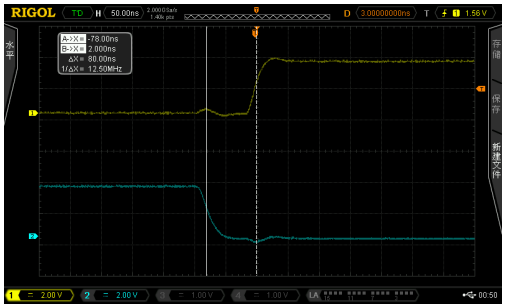

Figure 13. Dead band waveform of input signal(1)

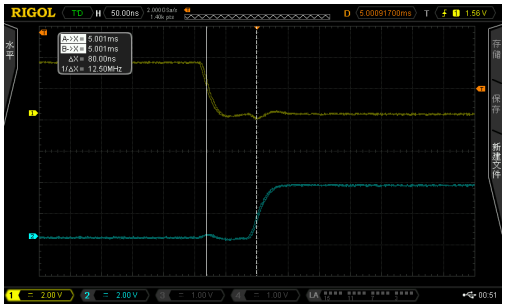

Figure 14. Dead band waveform of input signal(2)

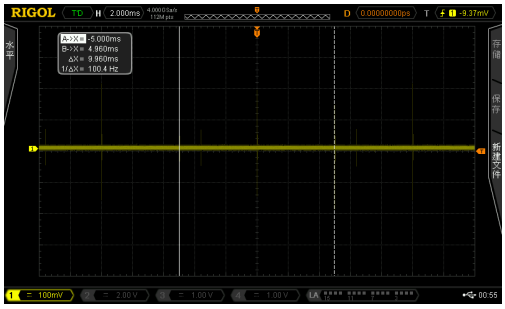

Figure 15. 100Hz echo signal

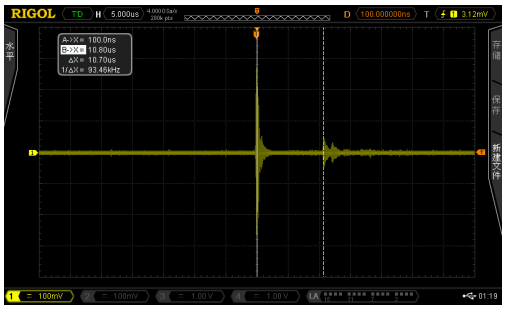

Figure 16. the first echo signal

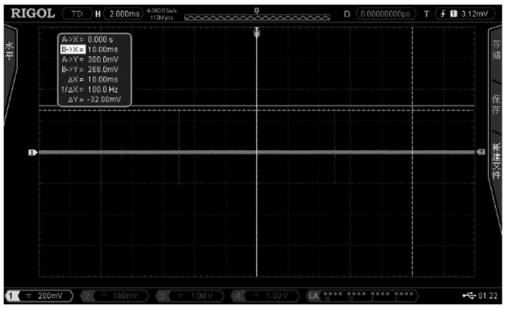

Figure 17. two echo signals

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4. Summary

Based on the background of ultrasonic defect detection, this paper analyzes the requirements of steel plate ultrasonic detection, and gives the specific design scheme. At the same time, the paper also gives a clear circuit design and implementation process. Firstly, the feasibility of the low-power excitation circuit based on half-bridge drive and bootstrap circuit is confirmed by the simulation analysis of the excitation circuit scheme. Through the specific design and experiment, the 200V high-voltage pulse, repetition rate and excitation voltage can be adjusted to excite the bicrystal ultrasonic probe. At the same time, if different voltage pulses are required, replace the MOSFET to meet the required voltage, as well as the DC-DC boost module and the double crystal probe that can meet different voltage requirements.

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