

Research on Dynamic Resource Allocation Strategy for Embedded FPGA Reconfigurable System Development Based on Innovation of Analog Mixed Signal Integrated Circuit and RF High Frequency Circuit Technology

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Abstract

In the context of the integration of semiconductor technology and intelligent systems, embedded FPGA reconfigurable systems have become a key carrier for innovation in analog mixed signal integrated circuits (AMS ICs) and RF circuits due to their flexibility and high performance. This article takes a management perspective and focuses on the dynamic resource allocation challenges of such complex R&D projects. By constructing a three-dimensional analysis framework of "technical characteristics resource requirements configuration mechanism" and combining typical cases in the semiconductor industry, a resource prediction model based on digital twins, a dynamic scheduling algorithm based on agile iteration, and an interdisciplinary knowledge network collaboration mechanism are proposed. Research has shown that the heterogeneity of analog mixed signals and RF high-frequency technology poses special requirements for the professional adaptability of R&D resources. The iterative development mode of reconfigurable systems requires real-time response capabilities for resource allocation, and the integration of digital twin technology and knowledge graph can effectively improve resource allocation efficiency. This study provides theoretical reference and practical path for resource management of high-tech R&D projects.

Keywords

Analog Mixed Signal Integrated Circuit; RF High-frequency Circuit; Embedded FPGA; Reconfigurable System; R&D Resources; Dynamic Configuration.

1. Introduction

1.1. Research Background

With the deep integration of 5G communication, the Internet of Things, and artificial intelligence, the research and development complexity of embedded FPGA reconfigurable systems, as a bridge connecting the digital and analog worlds, is growing exponentially. Especially the technological innovation of analog mixed signal integrated circuits (such as high-precision ADC/DAC) and RF high-frequency circuits (such as millimeter wave transceivers) has put forward multiple requirements for the reconfigurable architecture of embedded FPGAs, including low power consumption, high integration, and real-time performance. According to SEMI statistics, the global mixed signal IC market will reach \$42.7 billion in 2023, with a compound annual growth rate of 11.2%. The RF front-end market is expected to exceed \$35 billion by 2025, driven by 5G. This type of technology research and development has typical characteristics of "interdisciplinary intersection, high capital intensity, and long cycle iteration". Improper resource allocation will lead to low research and development efficiency - for example, a well-known semiconductor company extended the project cycle by 6 months and

increased costs by 15% due to delayed deployment of RF testing equipment in millimeter wave FPGA research and development. [1]

1.2. Research Significance

From a theoretical perspective, existing research on R&D resource allocation mostly focuses on a single technical field, lacking targeted analysis of analog digital hybrid systems. This study fills the theoretical gap in mixed signal and RF technology R&D management by constructing an interdisciplinary resource allocation theoretical framework. From a practical perspective, the dynamic allocation strategy of R&D resources for embedded FPGA reconfigurable systems can solve practical problems such as "heterogeneous technology collaborative development, scarce resource competition, and iterative demand response" for semiconductor enterprises. Especially in the current context of accelerated domestic chip substitution, improving resource allocation efficiency is of strategic significance for breaking through technological bottlenecks.

1.3. Research Framework

Adopting a progressive logic of "technical characteristic analysis → resource requirement modeling → configuration strategy design → case verification": firstly, analyzing the special requirements of the technical characteristics of analog mixed signals and RF high-frequency circuits for resource allocation; Secondly, construct a resource allocation model based on dynamic capability theory; Finally, the effectiveness of the strategy is verified by combining a 5G RF reconfigurable system development case from a certain FPGA manufacturer. [2]

2. Analysis of the Correlation between Technical Characteristics and R&D Resource Allocation

2.1. R&D Resource Requirements for Analog Mixed Signal Integrated Circuits

The analog mixed signal circuit combines the logic processing capability of digital circuits with the continuous signal processing capability of analog circuits. Its development process presents three major characteristics: 1. High precision testing equipment dependence: for example, dynamic characteristic testing of 16 bit or more ADCs requires the use of oscilloscopes with a sampling rate of $\geq 1\text{GS/s}$ and signal sources with an accuracy of $\pm 0.1\text{dB}$. Such equipment costs over one million US dollars per unit and requires regular calibration, forming a resource exclusive demand. 2. Cross domain knowledge fusion: Design engineers need to master both the timing analysis of digital circuits and the noise analysis methods of analog circuits. For example, in low-power ADC design, it is necessary to balance the power optimization of digital logic with the distortion control of analog front-end, and put forward composite requirements for the team's knowledge structure. 3. Iterative verification complexity: The simulation of mixed signal circuits requires the simultaneous operation of digital simulators (such as VCS) and analog simulators (such as Hspice), and collaboration through mixed signal simulation interfaces (such as Verilog AMS). A single complete simulation can take several hours, requiring extremely high parallel processing capabilities for computing resources. [3]

2.2. Special Characteristics of R&D Resources for RF High Frequency Circuits

The research and development of RF high-frequency circuits, especially in the millimeter wave frequency band, have unique resource requirements: 1. Special facility requirements such as microwave anechoic chambers: Antenna radiation characteristic testing of RF circuits above 30GHz must be conducted in microwave anechoic chambers, which have construction costs of tens of millions of yuan and require professional technical personnel to operate, forming regional resource barriers. 2. High frequency signal integrity challenge: The dielectric loss of PCB boards at high frequencies (such as $\tan \delta > 0.02$ at 10GHz for FR4) can significantly affect signal quality. The development process requires the collaboration of high-frequency

electromagnetic field simulation software (such as HFSS) and vector network analyzer (VNA), which imposes strict requirements on the accuracy of computing resources and testing equipment. 3. Investment of thermal management resources: The efficiency of RF power amplifiers (PA) in the millimeter wave frequency band is usually less than 30%. The heat dissipation design requires the support of thermal simulation software (such as Icepak) and thermal testing equipment (such as infrared thermal imagers), and the allocation of related resources directly affects the research and development progress.

2.3. Development Mode Transformation of Embedded FPGA Reconfigurable Systems

The "hardware and software" characteristics of reconfigurable systems have a profound impact on resource allocation: 1. Agile development requirements: FPGA based prototype validation allows for rapid iteration of hardware functionality (such as weekly version updates). The traditional waterfall style resource allocation model is difficult to adapt to, requiring dynamic adjustment of resource allocation for hardware design, software algorithms, and testing validation. 2. Heterogeneous computing resource integration: Reconfigurable systems often adopt a heterogeneous architecture of "CPU+FPGA+analog front-end". For example, the digital pre distortion (DPD) module of 5G base stations requires FPGA to implement algorithm acceleration, while coordinating with analog RF links, requiring real-time scheduling of cross domain resources. 3. Intellectual Property (IP) Reuse Characteristics: The reuse rate of analog mixed signal IP (such as PLL) and RF IP (such as LNA) directly affects R&D efficiency, and a dynamic management mechanism for IP resource pool needs to be established to avoid duplicate development. [4]

3. Theoretical Model Construction of Dynamic Allocation of R&D Resources

3.1. Analysis Framework Based on Dynamic Capability Theory

The dynamic capability theory emphasizes the ability of enterprises to integrate, construct, and restructure internal and external resources to adapt to rapidly changing environments. In the development scenario of embedded FPGA, dynamic configuration capability is reflected in three aspects:

Environmental perception capability: The impact of real-time monitoring technology iteration (such as the evolution of RF chips from Sub-6GHz to millimeter wave) and market demand (such as the demand for multi band RF reconfigurability in 5G base stations) on resource requirements, such as the need to quickly increase resource investment in millimeter wave testing equipment when the millimeter wave frequency band becomes mainstream.

Resource Refactoring Capability: Dynamically adjust resource combinations based on the R&D phase (conceptual design → RTL design → FPGA prototype → chip verification). For example, the conceptual phase focuses on algorithm engineers and system architects, while the chip stage requires an increase in the ratio of layout engineers to test engineers.

Organizational learning ability: Through cross project resource utilization data accumulation, optimize configuration strategies, such as extracting the empirical formula "every 10% increase in microwave anechoic chamber efficiency shortens project cycle by 1.5 months" from previous RF FPGA projects. [5]

3.2. Resource Demand Forecasting Model

Considering the particularity of simulating mixed signals and RF technology, a three-layer prediction model is constructed: 1. Technical parameter mapping layer: Establish a correlation matrix between technical indicators and resource requirements, for example, for every 1dB

increase in ADC signal-to-noise ratio (SNR), 2 high-precision oscilloscopes need to be used for longer periods of time; For every 10 GHz increase in the operating frequency of the RF circuit, the testing time in the microwave anechoic chamber increases by 30%.² Project Phase Evolution Layer: Based on SEI FPGA Development Maturity Model (FDMM), define resource requirement patterns for each stage:

Table 1. define resource requirement patterns for each stage

development phase	Core resource types	Resource characteristics
System definition	Architect, Market Analyst	Knowledge intensive, requiring cross disciplinary communication
RTL Design	FPGA engineer, analog circuit designer	Tool dependent (such as Vivado, ADS)
Prototype validation	Test engineer, FPGA development board	Equipment sharing type, requiring high-frequency debugging
Film production and mass production	Layout engineer, packaging testing equipment	Capital intensive, requiring dedicated facilities

3. Uncertainty buffer layer: Introducing Monte Carlo simulation processing technology risks, such as setting 15% -20% resource buffer in RF FPGA development to address iterations caused by high-frequency signal integrity issues.

3.3. Key Mechanisms of Dynamic Configuration

Digital twin driven resource simulation: Build a digital twin of R&D resources, including personnel skill matrix (such as engineers' proficiency in mixed signal simulation, RF matching network design, etc.), equipment state model (such as calibration cycle of vector network analyzer, usage period occupancy rate), and visualized prediction of resource usage through real-time data access.

The combination of Kanban method and constraint theory: Kanban management is used to visualize resource bottlenecks in the R&D process (such as scheduling conflicts in microwave darkrooms), while constraint theory (TOC) is applied to identify key resources (such as senior RF engineers), and non critical path resources are dynamically adjusted to ensure efficient utilization of bottleneck resources.

Knowledge graph assisted resource matching: Establish a knowledge graph of technical problems, experts, and tools. For example, when encountering the problem of "linearization of power amplifiers in millimeter wave FPGA", the system automatically matches engineers with DPD algorithm development experience and recommends using Keysight's PNA-X network analyzer and SystemVue simulation tool. [6]

4. Case Study: Research and Development Practice of 5G RF Reconfigurable System in a Certain FPGA Enterprise

4.1. Project Background and Challenges

A semiconductor company is developing a multi band RF reconfigurable FPGA system for 5G base stations, integrating a 28GHz millimeter wave RF front-end and reconfigurable digital baseband. The project has a duration of 24 months and a total budget of 120 million yuan. The core challenges include: simultaneously involving the Sub-6GHz and millimeter wave frequency bands below 6GHz, requiring a balance between research and development resources for low-frequency analog circuits and high-frequency RF circuits; Reconfigurable architecture requires hardware functionality to undergo more than 12 iterations during the FPGA prototype stage, which is difficult to cope with using traditional fixed resource allocation

models; There are multiple projects competing for key resources such as millimeter wave VNA (worth 8 million yuan) and microwave anechoic chambers (only 3 rooms).

4.2. Implementation of Dynamic Configuration Strategy

4.2.1. Resource Prediction based on Digital Twins

Build a digital twin model of the project, integrate 32 types of hardware resources (such as oscilloscopes and spectrometers) with the skill data of 56 R&D personnel into the middleware system, train LSTM neural network through historical project data, and achieve resource demand prediction for the next 4 weeks. For example, in the millimeter wave PA design phase, the system predicted the use conflict of a certain type of spectrometer, and allocated spare equipment in advance to avoid the proportion of waiting time from 35% to 8%.

4.2.2. Agile Iterative Resource Scheduling

Adopting the Scrum framework for iterative development, a resource coordination meeting is held before the start of each Sprint (2 weeks) to adjust resources based on the progress of the previous iteration: when the matching network design of the Sub-6GHz RF front-end is completed ahead of schedule, the originally planned 2 RF engineers will be promptly allocated to the millimeter wave link budget; In response to the signal integrity issue in FPGA prototype verification, we have temporarily increased the usage period of three high-speed oscilloscopes and improved equipment utilization to 92% through staggered scheduling (night use).

4.2.3. Construction of Interdisciplinary Knowledge Networks

Establish an enterprise level knowledge graph, integrate 1200+technical documents, 300+patents, and 200+project experience. When a team encounters eye diagram degradation problems in the high-speed serial interface design of millimeter wave FPGA, the system automatically pushes solutions similar to the case (such as optimizing PCB stack design to improve signal integrity in a project), and matches 3 engineers with high-speed circuit design experience to provide support, reducing the problem-solving time from 7 days to 3 days.

4.3. Evaluation of Implementation Effectiveness

Compared with the traditional resource allocation model, the implementation of dynamic strategies has significantly improved key indicators: 1 The R&D cycle has been shortened by 22%, from 24 months to 18.7 months; 2. The utilization rate of key equipment has increased by 37%, and the idle time of the microwave darkroom has been reduced from 15 hours per week to 5 hours; 3. Cross team collaboration efficiency increased by 41%, and knowledge reuse rate increased from 28% to 63%; 4. The R&D cost has been reduced by 19%, and the rental cost of testing equipment has decreased from 12 million yuan to 9.7 million yuan.

5. Design of Dynamic Resource Configuration Strategy for Embedded FPGA Reconfigurable System Development

5.1. Technical Heterogeneity Adaptation Strategy

A three-dimensional adaptation mechanism is proposed to address the cross domain characteristics of analog mixed signals and RF high-frequency technology.

Dynamic optimization of talent structure: Establish a matrix style talent pool of "basic skills+professional fields", requiring analog circuit engineers to master the basic analysis methods of RF circuits (such as S-parameters), RF engineers to understand the noise analysis of mixed signal circuits (such as PSRR), and cultivate composite talents through quarterly job rotation and cross project collaboration. For example, a certain enterprise implemented a "3+3" training program (3 months of analog circuit research and development+3 months of RF circuit research and development), which increased the efficiency of cross disciplinary problem solving by 58%.

Device resource sharing platform: Build a cloud based device sharing system to achieve remote calling and time-sharing reuse of high-precision testing equipment. For example, connecting multiple vector network analyzers distributed in different laboratories to a unified management platform, using intelligent scheduling algorithms to increase equipment utilization from 45% to 78%, while reducing downtime through remote calibration functions.

Dynamic management of IP resource pool: Establish standardized analog mixed signal IP and RF IP libraries, adopt version control and compatibility labeling, and recommend the most suitable IP combination through AI algorithms. For example, when designing a multi band RF FPGA, the system automatically recommends validated 28GHz LNA IP and 6GHz PA IP, and provides recommendations for their compatibility in terms of power domain isolation.

5.2. Iterative Development Response Strategy

To adapt to the agile development mode of reconfigurable systems, design a multi-layer response mechanism:

Elastic resource pool construction: Reserve 15% -20% of elastic resources, including backup FPGA development boards, temporary testing stations, and a cross domain engineer standby pool, to cope with unexpected demands during iterations. For example, when a timing issue is discovered between the RF front-end and FPGA interface during a certain iteration, the elastic resource pool can immediately allocate 2 timing analysis experts and 3 logic analyzers to avoid project delays.

Real time progress dashboard system: Develop a blockchain based R&D progress tracking platform, where module managers update task status in real-time, and the system automatically identifies resource bottlenecks and triggers alerts. For example, when the progress of the millimeter wave antenna design module lags behind by more than 3 days, the system automatically pushes an alert to the resource management committee and initiates the cross team resource allocation process.

Agile budget adjustment mechanism: Divide 30% of the total budget into a dynamic adjustment pool and allocate flexibly based on the actual needs of each iteration. For example, during the prototype verification phase, if it is found that the use of millimeter wave channel simulators needs to be increased, a special budget can be applied for from the dynamic pool to shorten the procurement approval cycle to 3 working days.

6. Conclusion and Prospect

6.1. Research Conclusion

This study constructs a targeted theoretical and methodological system for dynamic allocation of research and development resources by integrating the technical characteristics of analog mixed signals, RF high-frequency circuits, and embedded FPGA reconfigurable systems. The following core conclusions are drawn: 1 The heterogeneity of technology requires that resource allocation must take into account the professional characteristics of analog circuits and RF circuits, and achieve accurate prediction of cross domain resources through digital twin technology; The iterative development mode of reconfigurable systems requires the establishment of elastic resource pools and agile response mechanisms. The traditional fixed allocation mode can lead to resource waste of over 30%; The dynamic management of knowledge capital is the key to improving allocation efficiency, and cross project knowledge reuse can increase R&D efficiency by more than 40%.

6.2. Practical Insights

There are three inspirations for the R&D management practices of semiconductor enterprises: 1 At the strategic level, the ability to dynamically allocate resources will be incorporated into

the construction of the enterprise's core competitiveness, and a cross departmental resource management committee will be established to coordinate heterogeneous resources such as simulation, RF, FPGA, etc. 2. Tactical level: Invest in building a digital resource management platform that integrates personnel skills, equipment status, IP assets, and other data to achieve intelligent configuration decision-making. 3. Operational level: Implement the "Resource Agile Unit" model, break down large teams into cross disciplinary groups of 3-5 people, equip them with flexible and adjustable resource packages, and improve frontline response speed.

6.3. Future Outlook

Future research can be deepened in three aspects: 1 Deep integration of artificial intelligence: exploring the application of generative AI in resource allocation, such as automatically generating optimal resource combination solutions; 2. Green R&D considerations: Incorporate carbon emission indicators into resource allocation models, optimize the use of high energy consumption resources such as high-precision testing equipment; 3. Global resource collaboration: Study the dynamic allocation of resources for multinational R&D teams, and address new challenges such as time zone differences and cross-border flow of intellectual property. By continuously optimizing resource dynamic configuration strategies, the development of embedded FPGA reconfigurable systems will better support innovation in analog mixed signal and RF high-frequency technology, providing core technical support for the development of strategic fields such as 5G, 6G, and the Internet of Things.

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